Adapting Voltage Ramp-up Time for Temperature Noise Reduction on Memory-based PUFs

***Abstract*—The efficiency and cost of silicon PUF-based applications, and in particular key generators, are heavily impacted by the level of reproducibility of the bare PUF responses under varying operational circumstances. Error-correcting codes can be used to achieve near-perfect reliability, but come at a high implementation cost especially when the underlying PUF is very noisy. When designing a PUF-based key generator, a more reliable PUF will result in a less complex ECC decoder and a smaller PUF footprint, hence an overall more efficient implementation. This paper proposes a novel insight and resulting technique for reducing noise on memory-based PUF responses, based on adapting supply voltage ramp-up time to ambient temperature. Circuit simulations on 45nm Low-Power CMOS, as well as actual silicon measurements are presented to validate the proposed methods. Our results demonstrate that choosing an appropriate voltage ramp-up for enrollment and adapting it according to the ambient temperature at key-reconstruction is a powerful method which makes memory-based PUF response noise up to three times smaller.**

I. Introduction

In recent years, silicon *Physically Unclonable Functions* (PUFs) [1] have been well established as innovative hardware security primitives. Numerous constructions have been proposed and implemented (see, e.g., [2] for an overview), and their interesting properties are being extensively investigated in large scale experiments [3–5]. A silicon PUF's ability to generate device-unique fingerprints based on deep-submicron silicon process variations makes it a highly practical tool for device identification. In addition, the intriguing and unparalleled property of *physical unclonability* is a strong foundation for deploying a silicon PUF as a security primitive.

Combined with proper post-processing, a PUF is able to generate secret keys of cryptographic strength [6,7], and reliably store them in a highly secure manner without the need for conventional on-chip *Non-Volatile Memory* (NVM). The key is derived from the device-intrinsic randomness which is evaluated by the silicon PUF. The main purpose of a PUF-based key generator is twofold: *i)* increasing the *reproducibility* of a typically noisy PUF evaluation to near-perfect reliability, and *ii)* accumulating sufficient *unpredictability* of possibly low-entropic PUF responses into a highly unpredictable cryptographic key. It is evident that the natural reproducibility and unpredictability of a bare silicon PUF implementation have a strong impact on the efficiency, and hence on the cost of a PUF-based key generator as a whole. A PUF with less noisy and more random responses will result in a key generator which requires less "PUF material", and hence less silicon area, to produce a reliable cryptographic key.

To produce a key with a practically acceptable reliability level (e.g., failure rate $\leq 10^{-6}$), a PUF-based key generator based on a fuzzy extractor [8,9] uses *Error-Correcting Codes* (ECC) to correct noisy PUF responses.These ECC techniques are very effective in boosting the reliability but tend to be computationally intensive. Moreover, the helper data, which is an unavoidable byproduct of the fuzzy extractor, will partially disclose the unpredictability of the bare PUF responses. This needs to be compensated for by using more PUF material and hence a larger PUF. Both the complexity of the ECC decoder, and the amount of randomness loss due to the helper data, scale with the required error correction capability of the ECC, i.e. less reliable PUF responses will result in a more complex decoder and a larger silicon PUF footprint. Hence, there is a strong incentive to use a PUF construction with an as high as possible reproducibility of its bare responses. This objective is seriously complicated by the reproducibilty deterioration of silicon PUFs when subjected to varying operating conditions, like temperature and supply voltage variations.

Substantial research effort has been put into reliability enhancement of PUF-based key generators. Careful selection of the right ECC algorithms minimizes the helper data loss and decoder implementation cost [10,11]. On a physical level, construction improvements have been proposed to decrease the noise level of the bare silicon PUF responses directly, by modifying the PUF circuit [12,13] or the wafer mask set [14]. Analyzing a silicon PUF's susceptibility to its operating conditions has been explored for reliability enhancement [15,16].

In this work, we take this one step further by considering the combined effect of different operating parameters, in particular temperature and supply voltage ramp-up time, and their impact on the reproducibility of SRAM memory-based PUF responses. It is well known that temperature impacts the switching speed of electronic devices and contributes to electronic noise [3], whereas the voltage ramp-up time (i.e., the time it takes to reach the operational supply voltage after power-on) influences the power-up state of an SRAM [17,18]. This paper shows that intelligent matching of voltage ramp-up time to ambient temperature significantly improves the reproducibility of PUF responses at extreme temperatures, with noise levels up to 3× smaller than without matching. Moreover, this effective technique requires only a small number of additional building blocks and does not impose any modifications to the actual standard memory cell circuit. These effects are demonstrated, both in simulation and actual silicon measurements for SRAM PUFs [6,17], and in silicon only for other memory-based PUF types [19–22].

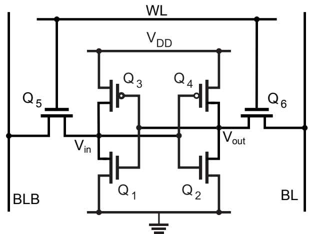

Fig. 1: SRAM Cell transistor level schematic.

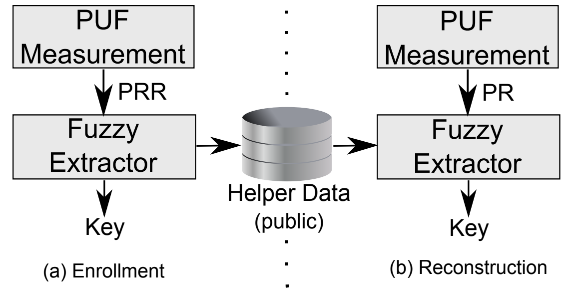

Fig. 2: Operations of a PUF based Key Storage System.

The remainder of this paper is organized as follows. Section II provides a brief background on memory-based PUFs and PUF-based key storage. Section III discuses the simulation setup, including the noise metric, and the simulation results. Section IV details the silicon measurement setup, including the optimization algorithms used and the achieved improvements. The obtained results are discussed in more detail in Section V, and Section VI provides possible implementation options. Finally, Section VII concludes the paper.

II. Background: PUFs and Key Generation

This section first briefly provide some preliminaries on the basic operation of memory-based PUFs. Then, it shows how PUFs are deployed in a key storage system, and thereafter it gives the PUF's main quality metrics.

A. Memory-based PUFs

Memory-based PUFs [6,19–22] comprise bistable circuits, i.e., having two possible stable states denoted as logic '0' and '1'. Fig. 1 shows a typical six-transistor SRAM cell with at its core a basic bistable circuit consisting of two cross-coupled inverters, respectively formed by (Q_1, Q_3) and (Q_2, Q_4). The peripherical circuitry used to access the cell is comprised by two pass transistors (Q_5 and Q_6), the bitline, the complement bitline and the wordline. When powered-up, the cross-coupled inverters start driving electric current, hence increasing the voltages at their gates (V_{in} and V_{out}). The first inverter that builds enough gate voltage to drive its NMOS (i.e., NMOS V_{th}) will pull-down its output, forcing the other inverter to pull-up and causing the SRAM cell to setlle in one of both stable states. Since both inverters are designed to be nominally identical, the outcome (in which of both states a cell settles) is entirely determined by the effect of random process variations. An SRAM cell power-up state is hence in effect a PUF response, and the corresponding construction is called an SRAM PUF [6].

B. PUF-based Key Generation and Storage

Fig. 2 shows the basic flow of a PUF-based key generation and storage system [6,7] based on a fuzzy extractor [8,9], which typically consists of two phases:

(a) **Enrollment:** a key is generated from a *PUF Reference Response* (PRR) as shown in Fig. 2(a). First, the PUF is evaluated and produces the PRR. Next, the PRR is processed by the fuzzy extractor into a cryptographically strong key, and helper data is generated as a byproduct of the fuzzy extractor's internal ECC method. Finally, the helper data is stored in an external NVM (and hence becomes public information).

(b) **Reconstruction:** the earlier enrolled key is reliably recovered from a noisy *PUF Response* (PR) and the stored helper data as shown in Fig. 2(b). First, the PUF is evaluated again and produces the noisy PR. Next, PR is processed by the fuzzy extractor in combination with the helper data which is retrieved from the external NVM. If the noisy PR is close enough to the PRR obtained during enrollment (i.e. the PUF response is reproducible upto a limited amount of noise), then the extractor succeeds in reliably reconstructing the enrolled key.

C. PUF Properties

The two most basic quality measures of a PUF implementation are *reproducibility*: expressing how reliable a response can be reproduced on a single device, and *uniqueness*: expressing the difference between responses coming from distinct devices.

1) Reproducibility: A fuzzy extractor needs to be designed to cope with the worst-case expected difference between PRR at enrollment and PR at reconstruction in order to obtain a reliable key generation. The noise on a PUF response is typically expressed as the relative number of bit flips between the enrollment PRR and the PR during reconstruction. The smaller the expected noise, and hence the higher the *reproducibility* of the PUF responses, the more efficient the overall PUF-based key generation system can be implemented.

2) Uniqueness: To generate a secure key, a fuzzy extractor requires that a PUF response is unpredictable, even when other responses on the same PUF or access to other PUFs are given. This entails that:

- The probability that two different PUFs have responses close to each other should be negligible, i.e., PUF responses are highly *unique* and the expected amount of differing bits is close to 50%.
- The bits in a specific PUF response should be highly random and independent, i.e., each bit provides a negligible amount of information about the remaining response bits, and the relative entropy of each response is large.

III. Simulations

A memory system comprising a cell and peripheral circuitry is synthesized and simulated using SPICE, to analyze the

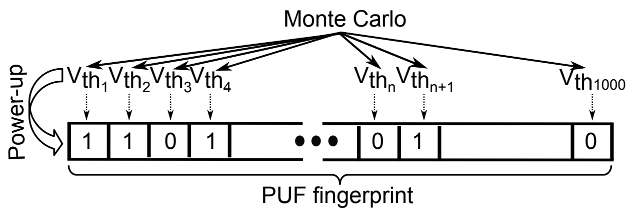

Fig. 3: SRAM PUF simulation.

reproducibility of memory-based PUFs by adapting the voltage ramp-up time to the environmental temperature. In this section, first, the PUF fingerprint generation is presented. Second, the metric used to evaluate noise is discussed. Finally, simulation experiments and results are described.

A. SRAM PUF Response Simulation

Each bit of an SRAM PUF response is generated by an individual SRAM cell. Fig. 3 shows the SRAM fingerprint generation schematic used in our simulations. It has been shown in [17] that the threshold voltage V_{th} of NMOS transistors is the technology parameter with the most impact on the start-up value of an SRAM cell. Hence, Monte Carlo method is used to generate 1000 random values of V_{th} for Q_1 (see Figure 1) according to the distribution presented in [23], i.e., mean μ = standard NMOS V_{th} and deviation σ = $9\% \cdot \mu$. These 1000 SRAM cells combined create an SRAM cell array that generates a unique and random 1000-bit response after power-up.

B. Noise Metric

To analyze the noise we read the PR of the simulated SRAM cell array for different voltage ramp-up times (t_{ramp}) and different temperatures (*Temp*). Then, the *Fractional Hamming Distance* (FHD) of each measured response compared to the enrollment response (PRR) is calculated; this is the number of differing bits normalized to the response length.

C. Simulation Experiments

To investigate the impact of the voltage ramp-up time t_{ramp} on the noise at different temperatures *Temp*, we consider a range of values for both t_{ramp} and *Temp* for 45nm *Low Power* (LP) [24]. For each combination of *Temp* and t_{ramp} we simulated the power-up of the SRAM cell array 20 times and read its response. The transient noise during power-up is randomly generated by the simulation tool, hence three variable parameters are used for the simulation:

- **Voltage ramp-up time:** $3\times t_{ramp}$ ($10\mu s$, $50\mu s$ and $90\mu s$),
- **Temperature:** $3 \times$ *Temp* (-40°C, $+25$°C, $+85$°C) and,
- **Measurements:** $20 \times$ *Meas* (each with a random seed).

Hence, a total of $(3 \times t_{ramp}) \times (3 \times Temp) \times (20 \times Meas) \times (1000 \times V_{th}) = 180{,}000$ simulations are performed.

D. Simulation Results

Fig. 4 shows the results of FHD calculations per t_{ramp} and $Temp$ considering enrollment performed at $+25$°C with t_{ramp} of (a) 10μs, (b) 50μs and (c) 90μs.

TABLE I: Description of devices used in validation.

Technology	# ICs	# PUF inst. / IC			Total # PUF inst.		
		BK	DFF	SRAM	BK	DFF	SRAM
40nm LP	5	-	-	3	-	-	15
65nm LP	50	2	4	4	100	200	200
130nm LP	16	-	1	1	-	16	16

From Fig. 4(a) it can be seen that for *Temp* below the enrollment ($+25$°C), $\max$ FHD is lower if t_{ramp} is longer than the one used for enrollment. However, at *Temp* above the enrollment, the opposite is true, e.g., at $+85$°C, key-reconstruction with $10\mu s$ generates the lowest $\max$ FHD while at -40°C, that is true for $90\mu s$.

Fig. 4(b) and (c) report similar results but now for other t_{ramp} at enrollment ($50\mu s$ and $90\mu s$). Following the trend observed previously, for *Temp* below enrollment ($+25$°C), $\max$ FHD is lower if t_{ramp} is longer than the one used during enrollment; e.g., considering Fig. 4(b), at $+85$°C, key-reconstruction with $10\mu s$ generates the lowest $\max$ FHD while at -40°C, that is true for $90\mu s$.

IV. Silicon Validation

The theoretical results from the simulations are validated in an experiment using silicon devices. For this purpose, measurements are performed on three different types of memory-based PUFs: the SRAM PUF [6,17], the D flip-flop (DFF) PUF [20] and the buskeeper (BK) PUF [21].

A. Test Set-up

The considered memory-based PUF types are manufactured in three different LP technology nodes. Table I provides an overview of all devices citing the technology node, the number of available integrated circuits (ICs), the number of PUF instances per IC in the given technology (if any), and the total number of tested instances of each PUF type. Note that each IC contains one or more PUF instances.

Measurements are performed at three different temperatures (-40°C, $+25$°C and $+85$°C)[1] and for ten different t_{ramp} varying from $10\mu s$ to $500ms$. In case of the 40nm SRAM, the shortest possible t_{ramp} is $50\mu s$ due to specific capacitive load. The measurements flow is as follows:

1) The ICs are placed in a climate chamber and connected to a programmable power supply.
2) Climate chamber is set to one of the test temperatures.
3) ICs are powered with a t_{ramp} from the test set.
4) Each PUF device response is read and stored in a file.
5) The ICs are powered down for 1 second.
6) Steps 3 to 5 are repeated 9 times (i.e. 10 measurements per PUF per temperature per t_{ramp}).
7) Change t_{ramp} and repeat steps 3 to 6 (until all values of t_{ramp} have been tested for this temperature).
8) Change temperature and repeat steps 3 to 7.

[1] Industrial standard for temperature testing of ICs ranges from -40°C to $+85$°C, which are therefore part of the test as worst case temperatures in comparison to the enrollment temperature of $+25$°C.

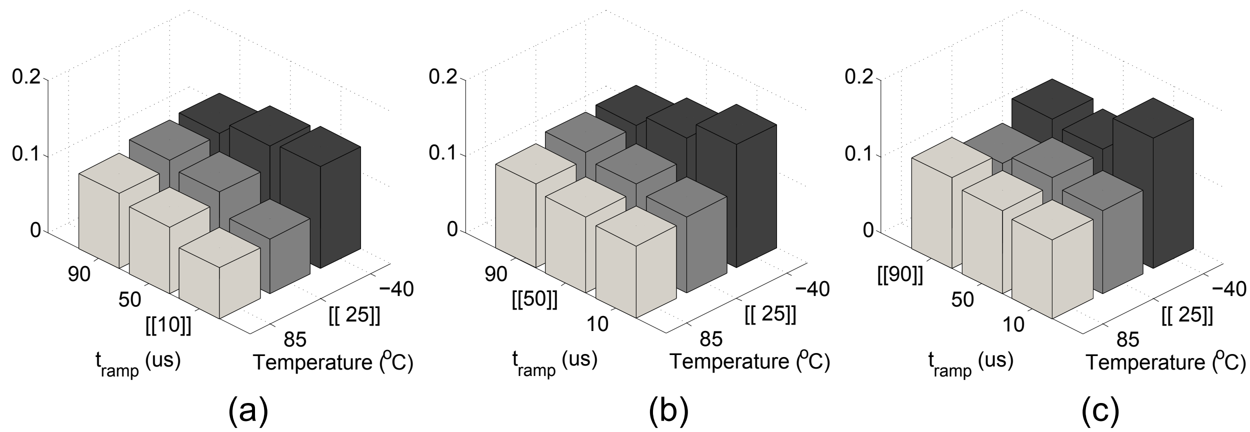

Fig. 4: Maximum Fractional Hamming Distance ($\max$ FHD); enrollment performed at $+25°$C with t_{ramp} of (a) 10μs, (b) 50μs and (c) 90μs.

B. Evaluation Metrics

1) Reproducibility: For calculating FHD, first an enrollment response of each PUF instance is measured. Thereafter, each reconstruction measurement is compared to this enrollment by counting the number of flipped bits and dividing it by the response length. A key based on the PUF response (as described in Section II) is reliable if the worst-case FHD under any stress condition is below the error correction capability of the ECC. Hence, the smaller FHD (noise), the lower the required error correction.

2) Uniqueness: We evaluate the uniqueness of the different PUF implementations by considering *(a)* the *average between-class Hamming distance* (μ-BCHD), and *(b)* the estimated *min-entropy* (H_∞) of the measured responses. Note that the uniqueness is analysed only at enrollment. In the key storage use case (as described in Section II) only the uniqueness of the enrollment PUF response is critical, as it is from this response that the cryptographic key is derived.

μ-BCHD provides an indication of uniqueness. This value is calculated as follows:

1) The enrollment response of each PUF is measured.
2) The Hamming distance between each pair of enrollment responses coming from different PUF instances of the same type is determined (e.g. between all pairs of enrollment responses of 65nm LP SRAM PUFs are computed).
3) The distribution of these *between-class* distances is determined and the obtained mean value, normalized to the response length, is μ-BCHD.

Optimally, the obtained distribution should be approximately Gaussian and μ-BCHD should be very close to 50% [17].

Min-entropy is used to evaluate the intrinsic unpredictability of the PUF responses. Min-entropy is a pessimistic measure of the unpredictability of a random variable [8]. We estimate the min-entropy of the responses of a particular PUF type by considering the following model: each PUF response bit is independent of the other bits in the same response and has an individual probability p_1 of being '1' for a random PUF instance. This model is particularly reasonable for memory-based PUFs, as each response bit originates from an individual memory cell. Under the assumption of this model, the min-entropy of a single response bit is calculated as $H_\infty = -\log_2 \ \max\{p_1, 1-p_1\}$. The value for p_1 of a bit is estimated by counting the number of enrollment responses for which this bit is '1' and dividing by the total number of enrollment responses. The min-entropy of the entire response is simply the summation of the min-entropy of each bit. We express H_∞ as the average min-entropy per bit in a response value, by dividing the total min-entropy of the response by its length. Optimally, H_∞ of a PUF response bit should be close to 1. Note that, due the limited number of measured PUF instances, the obtained estimations of H_∞ could be smaller than the actual min-entropy of these PUF responses.

C. Optimization Algorithms

The silicon test analyses have the objective to investigate the use of t_{ramp} as a technique for increasing memory-based PUF response reproducibility (noise reduction). As a side effect, the impact on PUF uniqueness is also investigated. For this purpose, two optimization algorithms are used:

1) Reproducibility optimization: This algorithm identifies for each value of t_{ramp} at enrollment the t_{ramp} configuration per temperature that leads to the highest reproducibility (lowest maximum noise) at extreme temperatures.

2) Uniqueness optimization: This algorithm identifies the enrollment t_{ramp} that provides the highest H_∞. After this first step the values of t_{ramp} at other temperatures are determined, which minimize the noise.

D. Measurement Results

In order to evaluate the performance of the optimization algorithms, the original PUF measurements (without optimization) need to be analysed first. Table II shows the original measured maximum noise values for the considered temperatures as well as uniqueness indicators. These values are obtained using the shortest possible t_{ramp} for each PUF. As stated before, the noise is determined using 10 response measurements per PUF per temperature.

TABLE II: Measurement results without optimization.

Technology	**PUF**	t_{ramp}	**Maximum noise FHD**			μ-BCHD	H_∞
			$-40°$C	$+25°$C	$+85°$C		
40nm LP	SRAM	50μs	23%	6%	20%	0.50	0.73
65nm LP	SRAM	10μs	8%	6%	8%	0.50	0.87
	DFF	10μs	28%	8%	25%	0.37	0.40
	BK	10μs	10.5%	4.5%	20%	0.48	0.75
130nm LP	SRAM	10μs	13%	6%	12%	0.47	0.66
	DFF	10μs	16.5%	5%	28%	0.43	0.61

Table II reveals that overall the maximum noise measured at $-40°$C is 28% (for the 65nm DFF PUF), at $+25°$C is 8% (for the 65nm DFF PUF), and at $+85°$C is 28% (for the 130nm DFF PUF). Regarding uniqueness, although a truly fair comparison is not possible due to the different number of devices available per technology node and PUF type, the 65nm DFF PUF has the lowest μ-BCHD $= 0.37$ and $H_\infty = 0.40$.

1) Reproducibility optimization: Table III presents the results of the reproducibility optimization algorithm; it shows the t_{ramp} configuration that minimizes the noise (maximizes the reproducibility) per temperature in comparison to the enrollment. The results show that for all tested PUFs, adapting t_{ramp} to the ambient temperature has a major impact on the maximum noise. For low temperatures, noise reduction is realized with longer t_{ramp}; whereas for high temperatures, this is realized with shorter t_{ramp}; e.g., the maximum noise for the 65nm LP DFF PUF at $-40°$C with $t_{ramp} = 10\mu s$ for both enrollment and reconstruction was originally 28%. If the optimized t_{ramp} is used both at the enrollment ($500\mu s$ at $+25°$C) and at reconstruction ($50ms$ at $-40°$C), then the maximum noise is reduced to merely 11.5%. Note that all results in Table III demonstrate the *same trend* as predicted by the simulation results of Section III-D. Since this algorithm does not optimize the uniqueness, μ-BCHD and H_∞ decrease for some PUFs (e.g. the 130nm SRAM PUF), while they increase for others (e.g. the 65nm DFF PUF).

2) Uniqueness optimization: Table IV reports the results of the uniqueness optimization algorithm; it shows *(a)* the t_{ramp} at enrollment that maximizes uniqueness and *(b)* the t_{ramp} for the other temperatures that results in the lowest maximum noise (with respect to the t_{ramp} selected for enrollment). Uniqueness indicators μ-BCHD and H_∞ are at least as high as the originals for 40nm and 130nm SRAMs, and for the remaining devices these indicators are higher than the original indicators. The uniqueness optimization algorithm clearly leads to significant improvements in μ-BCHD and H_∞ for the tested DFF and buskeeper PUFs. Improvements for the SRAM PUFs from all tested nodes are negligible. Since this algorithm does not select the enrollment t_{ramp} optimized for reproducibility, it is natural that the noise resulting from this algorithm is worse than that of reproducibility optimization algorithm. In case of the 65nm SRAM PUF, the maximum noise at $-40°$C is even worse than the measurements without optimization. Reason for this is that the t_{ramp} at enrollment ($+25°$C) is very long and the algorithm is unable to find a corresponding longer t_{ramp} at $-40°$C.

TABLE III: Results after reproducibility optimization.

Technology	**PUF**	t_{ramp}			**Maximum noise FHD**			μ-BCHD	H_∞
		$-40°$C	$+25°$C	$+85°$C	$-40°$C	$+25°$C	$+85°$C		
40nm LP	SRAM	10ms	1ms	50μs	14%	4.5%	17%	0.49	0.71
65nm LP	SRAM	50ms	250μs	10μs	7%	5.5%	7%	0.50	0.89
	DFF	50ms	500μs	25μs	11.5%	5%	9%	0.49	0.84
	BK	500ms	1ms	25μs	6.5%	4%	6.5%	0.46	0.69
130nm LP	SRAM	500ms	10ms	1ms	5.5%	2%	5%	0.37	0.42
	DFF	500ms	10ms	500μs	12.5%	2.5%	8.5%	0.45	0.67

TABLE IV: Results after uniqueness optimization.

Technology	**PUF**	t_{ramp}			**Maximum noise FHD**			μ-BCHD	H_∞
		$-40°$C	$+25°$C	$+85°$C	$-40°$C	$+25°$C	$+85°$C		
40nm LP	SRAM	1ms	100μs	50μs	16%	6%	19%	0.50	0.73
65nm LP	SRAM	50ms	100ms	50μs	13%	2%	8%	0.50	0.89
	DFF	500ms	10ms	250μs	18.5%	2.5%	8%	0.50	0.90
	BK	100ms	250μs	10μs	7%	5%	9%	0.50	0.88
130nm LP	SRAM	1ms	10μs	10μs	7.5%	6%	12%	0.47	0.66
	DFF	50ms	500μs	10μs	10%	4.5%	9.5%	0.47	0.67

V. Discussion

SPICE simulations show that using long t_{ramp} at low temperatures and short t_{ramp} at high temperatures results in reduced SRAM PUF response noise when compared to enrollment. The observation is validated using silicon measurement, and regardless of the technology node and memory PUF type. Hence, choosing appropriate t_{ramp} according to ambient temperature, including enrollment, can be used as an efficient scheme to reduce noise and increase reproducibility.

Moreover, the silicon measurements have also indicated that varying the voltage ramp-up time can have a significant impact on the uniqueness of memory-based PUFs. By choosing the appropriate optimization algorithm according to the PUF type, noise can be reduced while either maintaining or increasing the uniqueness indicators. Inspecting the silicon results with regard to reproducibility and uniqueness we conclude the following:

- SRAM PUFs benefit from applying the reproducibility optimization algorithm, but the uniqueness optimization algorithm is not very effective as there is very little margin for improvement. Furthermore, the uniqueness optimization algorithm does not minimize the noise well for the tested SRAMs.
- Buskeeper and DFF PUFs benefit from applying the uniqueness optimization algorithm, since the original silicon results show that there is a lot of room for improvement. Besides increasing the PUF response uniqueness, the proposed algorithm also decreases the noise at extreme temperatures. Hence, this algorithm works very well for these PUF types.

VI. Implementation Considerations

The proposed scheme can be implemented by a simple circuit consisting of a voltage regulator and a temperature

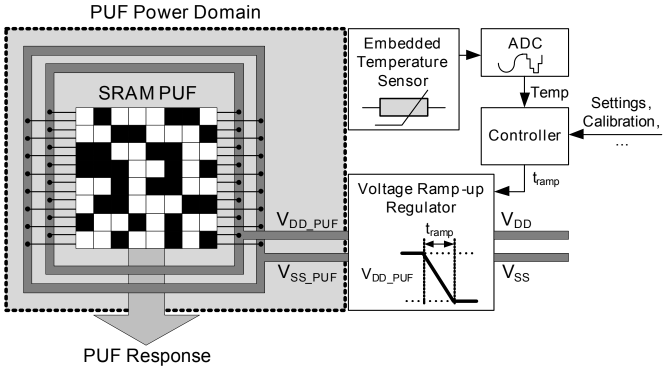

Fig. 5: Schematic of an extended SRAM PUF design.

sensor. Fig. 5 shows an example of such a circuit, comprising five blocks, an SRAM PUF, a voltage ramp-up regulator, an embedded temperature sensor, an ADC and a controller.

The circuit performs five main steps. First, the temperature sensor senses the ambient temperature. Second, this temperature is used as an input to the ADC that converts the given temperature to the closest digital temperature *Temp*. Third, according to *Temp* the Controller is calibrated and the t_{ramp} that minimizes the FHD (noise) is produced. Fourth, the voltage ramp-up regulator powers-up the SRAM PUF with the assigned t_{ramp} and finally, the SRAM PUF generates a PUF response.

One of the main advantages of the proposed optimization technique, besides its evident effectiveness, is that its implementation demands no adaptations of the memory-based PUF circuit itself. In fact the basic PUF comprises only standard library memory cells, but needs to be placed in its own power domain and extended with an embedded temperature sensor and a voltage ramp-up regulator. A small controller regulates the optimal ramp-up time of the memory-based PUF to the sensed temperature, based on a prior calibration. The general design of these extensions is schematically shown for an SRAM PUF in Fig. 5. Since the concerned building blocks are all rather standard, the implementation effort of the proposed optimization technique is considered minimal, in particular in relation to the large obtained gain in PUF reproducibility as demonstrated in Section IV.

VII. Conclusion

In this paper, we proposed a method based on adapting the voltage ramp-up time to the ambient temperature for enhancing the reproducibility of memory-based PUFs. The combined effect on PUF reproducibility has been evaluated using both circuit simulation (in 45nm LP CMOS) and actual silicon measurements (in 45nm, 65nm and 130nm LP CMOS). The results are highly effective, showing a major decrease in worst-case PUF noise (up to 3× lower for particular PUFs) at extreme temperatures. A significant advantage of the proposed noise-reduction technique is that it can be implemented without altering existing memory-based PUF circuits, but merely by extending them with some relatively standard building blocks. The application of the proposed techniques will result in a significantly reduced complexity and a smaller footprint of a PUF-based key generator. The reproducibility enhancement is achieved while either mantaining or increasing the uniquess. Future work will include investigating the proposed techniques for alternative memory-based PUFs and other silicon technologies, and implementing the extensions to enable them in silicon.

References

[1] B. Gassend, D. Clarke, M. van Dijk and S. Devadas, "Silicon physical random functions", *ACM CCS*, pp. 148–160, 2002.
[2] R. Maes and I. Verbauwhede, "Physically Unclonable Functions: A Study on the State of the Art and Future Research Directions", *Towards Hardware-Intrinsic Security*, A.-R. Sadeghi and D. Naccache (Eds.), pp. 3–37, 2010.
[3] S. Katzenbeisser, Ü. Kocabas, V. Rozic, A.-R. Sadeghi, I. Verbauwhede and C. Wachsmann, "PUFs: Myth, Fact or Busted? A Security Evaluation of Physically Unclonable Functions (PUFs) Cast in Silicon", *CHES*, pp. 283–301, 2012.
[4] A. Maiti, J. Casarona, L. McHale and P. Schaumont, "A large scale characterization of RO-PUF", *HOST*, pp. 94–99, 2010.
[5] T. Yoshida, T. Katashita and A. Satoh, "Quantitative and Statistical Performance Evaluation of Arbiter Physical Unclonable Functions on FPGAs", *ReConFig*, pp. 298–303, 2010.
[6] J. Guajardo, S.S. Kumar, G.-J. Schrijen and P. Tuyls, "FPGA Intrinsic PUFs and Their Use for IP Protection", *CHES*, pp. 63–80, 2007.
[7] B. Skoric, P. Tuyls and W. Ophey, "Robust key extraction from Physical Unclonable Functions", *ACNS*, pg. 99–135, 2005.
[8] Y. Dodis, L. Reyzin and A. Smith, "Fuzzy extractors: How to generate strong keys from biometrics and other noisy data", *SIAM Journal on Computing*, pp. 97–139, 2008.
[9] J.-P. Linnartz and P. Tuyls, "New shielding functions to enhance privacy and prevent misuse of biometric templates", *AVBPA*, pp. 393–402, 2003.
[10] R. Maes, A. Van Herrewege and I. Verbauwhede, "PUFKY: A Fully Functional PUF-Based Cryptographic Key Generator", *CHES*, pp. 302–319, 2012.
[11] V. van der Leest, B. Preneel and E. van der Sluis, "Soft Decision Error Correction for Compact Memory-Based PUFs Using a Single Enrollment", *CHES*, pp. 268-282, 2012.
[12] M. Hofer and C. Boehm, "An Alternative to Error Correction for SRAM-Like PUFs", *CHES*, pp. 335–350, 2010.
[13] V. Vivekraja and L. Nazhandali, "Circuit-level techniques for reliable Physically Uncloneable Functions", *HOST*, pp. 30–35, 2009.
[14] D. Forte and A. Srivastava, "On improving the uniqueness of silicon-based physically unclonable functions via Optical Proximity Correction", *DAC*, pp. 96–105, 2012.
[15] M. Bhargava, C. Cakir and K. Mai, "Attack Resistant Sense Amplifier based PUFs (SA-PUF) with Deterministic and Controllable Reliability of PUF Responses", *HOST*, pp. 106–111,2010.
[16] R. Kumar, H.K. Chandrikakutty and S. Kundu, "On improving reliability of delay based Physically Unclonable Functions under temperature variations", *HOST*, pp. 142–147, 2011.
[17] D.E. Holcomb, W.P. Burleson and K. Fu, "Power-Up SRAM State as an Identifying Fingerprint and Source of True Random Number", *IEEE Transactions on Computers*, vol. 58, no. 9, 2009.
[18] M. Claes, V. van der Leest and A. Braeken, "Comparison of SRAM and FF PUF in 65nm technology", *NordSec*, pp. 47–64, 2011.
[19] S.S. Kumar, J. Guajardo, R. Maes, G.-J. Schrijen and P. Tuyls, "The Butterfly PUF protecting IP on every FPGA", *HOST*, pp. 67–70, 2008.
[20] R. Maes, P. Tuyls and I. Verbauwhede, "Intrinsic PUFs from Flip-Flops on Reconfigurable Devices", *WISSec*, 2008.
[21] P. Simons, V. van der Leest and E. van der Sluis, "Buskeeper PUFs, a promising alternative to D Flip-Flop PUFs", *HOST*, pp. 7–12, 2012.
[22] Y. Su, J. Holleman and B. Otis, "A 1.6pJ/bit 96% Stable Chip-ID Generating Circuit using Process Variations", *ISSCC*, pp. 406–611, 2007.
[23] W. Zhao, F. Liu, K. Agarwal, D. Acharyya, S.R. Nassif, K.J. Nowka and Y. Cao, "Rigorous extraction of process variations for 65nm CMOS design", *ESSDERC*, pp. 89–92, 2007.
[24] "http://ptm.asu.edu/", 2012.